CLAIM

1. A method of forming wafer level package for producing a chip size packaging, said method comprising:

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providing a plurality of dies on the wafer, wherein said wafer has I/O metal pads on a first surface of said wafer;

coating a photo sensitive polymer on said first surface;

removing a portion area of said photo sensitive polymer to expose said metal pad;

coating a photoresist on a second surface of said wafer;

forming a first conductive layer in said photo sensitive polymer and covering said metal pad;

forming a conductive seeding layer on the top of said first conductive layer and said photo sensitive polymer;

patterning a photoresist on the top of said seeding layer to define circuit pattern;

forming a second conductive layer on said defined photoresist pattern to serve as the circuit distribution diagram;

removing said photoresist pattern, and removing the seeding layer covered by said photoresist pattern;

forming trenches in between of the packaging entity;

filling material in said trenches and covering said circuit distribution diagrams;

grinding said second surface of said wafer until said filling material is exposed;

executing an opening step to expose a portion of said circuit distribution diagram to define a reserved area for a conductive bump;

executing a solder screen printing step to form a layer of solder on said reserved area; and

reflow said solder to form a conductive bump.

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2. The method according to claim 1, wherein after executing said reflowing process, further comprising testing said wafers.

3. The method according to claim 2, wherein after executing said testing, further comprising a cutting process along said trenches.

4. The method according to claim 1, wherein said photo sensitive polymer comprises photo PI.

5. The method according to claim 1, wherein said photo sensitive polymer comprises EPOXY.

6. The method according to claim 1, wherein said opening of said metal pad is formed by laser.

7. The method according to claim 1, wherein said first conductive layer comprises alloy with the composition of Zn/Ni/Cu.

8. The method according to claim 1, wherein the formation of said seeding layer is formed by using electroless copper plating.

9. The method according to claim 1, wherein said second conductive layer comprises copper.

10. The method according to claim 9, wherein said copper is formed by electroplating.

11. The method according to claim 1, wherein said filling material comprises EPOXY.

12. The method according to claim 1, further comprising a step to solidify said EPOXY.

13. A wafer level package comprising:

a plurality of chips on a wafer, said wafer has trench formed in said wafer and run through said wafer;

material filled in said trenches;

metal pad formed on the surface of said wafer;

photo sensitive polymer material formed on the surface of said wafer and expose said metal pad;

a first conductive layer formed within said photo sensitive polymer material;

circuit diagram patterning formed on the top of said photo sensitive polymer material and said first conductive layer;

a protection layer covered on said circuit diagram, said photo sensitive polymer material and a portion of said circuit diagram exposed; and

a conductive bump formed on said exposed circuit diagram.

14. The wafer level package according to claim 13, wherein said photo sensitive polymer comprises EPOXY.

15. The wafer level package according to claim 13, wherein said photo sensitive polymer comprises photo PI.

16. The wafer level package according to claim 13, wherein said filling material comprises EPOXY.

17. The wafer level package according to claim 13, wherein said protection layer comprises EPOXY.

18. The wafer level package according to claim 13, wherein said conductive pattern diagram comprises copper.

19. The wafer level package according to claim 13, wherein said conductive bump comprises solder.

WAFER LEVEL PACKAGE AND THE PROCESS OF THE SAME

The present invention uses wafer level package method. This invention also provides a wafer level package method suit for the wafer level packaging test. The packaging step is conducted before cutting the wafers. The wafer level package comprising: a plurality of dies formed on the wafer, an I/O metal pad formed on the first surface of the wafer. Then, coating a photo sensitive polymer, for example, photo PI on the first surface, then a portion of the film is removed by laser. In the next step, coating a first photoresist on the second surface of the wafer, said first photoresist comprising positive photoresist. Forming a first conductive layer in the hole (opening) of the photo sensitive PI and then covering a metal pad, the first conductive layer comprising alloy with the composition of Zn/Ni/Cu. In the next step, forming a seeding layer with copper on the top of the first conductive layer and the photo sensitive polymer. Then, forming a second photoresist on the seeding layer to define the circuit pattern diagram. Then, forming a second conductive layer to the circuit pattern diagram located on the defined are of the second photoresist. The second conductive layer comprises copper. Removing the second and the first photoresist and the seeding layer covered by the second photoresist, thus forming trenches between each of the packaging entity. Then, the filling material was filled into the trench and covers the circuit pattern diagram. The filling material comprises EPOXY. Then, executing the grinding process to grind the

second surface of the wafer to expose the filling material. Next, executing an opening step to expose a portion of the circuit pattern diagram to define an area formed by the conductive convex block. Executing a solder screen printing step to form a solder area, then reflowing this area to form a conductive bump.